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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/746,459	12/26/2000	Eung-Youl Kang	P66216US0	2398

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EXAMINER

FARAHANI, DANA

ART UNIT

PAPER NUMBER

2814

DATE MAILED: 06/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/746,459

Applicant(s)

KANG, EUNG-YOUL

Examiner

Dana Farahani

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 March 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (U.S. Patent 5,023,694), previously cited, in view of Kenney (U.S. Patent 5,640,030), all previously cited.

Yeh discloses, figures 3 and 4, a memory cell comprising a first active area, parts of region 16, incorporating therein a gate of a depletion mode transistor 44; a second active area, other parts of region 16 that are not included in the first active area, adjacent to the first active area and incorporating therein a gate of an enhancement mode transistor 38; a word line, shown as V_{WL} and V_{FG} , coupled to the gate of the depletion mode transistor 44 and the gate of the enhancement mode transistor 38; a capacitor C_s coupled to a drain of the enhancement mode transistor 38.

Yeh does not disclose the capacitor being ferroelectric, and one of the capacitor's terminal is connected to a cell plate for storing data.

Kenney discloses in figure 1 a RAM memory cell, wherein the ferroelectric capacitors shown as FC are connected between plates P and source/drain of transistors S in order to store and retrieve data in plate lines (see column 2, line 41; column 5, lines 66 and 67; and column 6, lines 1-25). Therefore, it would have been obvious to one of

Art Unit: 2814

ordinary skill in the art at the time of the invention to include the cell plate in Yeh's structure in order to be able to store, and retrieve, data in the capacitors shown in figure 3 of Yeh's invention.

3. Claims 2, 3, and 5-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh in view of Kenney, as applied to claim 1 above, and further in view of Hoffman (U.S. Patent 4,486,859), previously cited.

Regarding claims 2, 3, 5-8, and 10-13, Yeh in view of Kenney renders obvious the claimed invention, as discussed above, but does not disclose the first active area of the memory cell is coupled to first active areas of neighboring memory cells. Hoffman discloses, figure 1, the first active area C2 of memory cell 10 is coupled to first active areas of neighboring memory cells (only one of them shown in the figure, below memory cell 10). Therefore, it would have obvious to one of ordinary skill in the art at the time of the invention to include this limitation in Yeh's structure in order to form an array of memory cells (note that in claim 5, although not shown explicitly a common cell plate, but Plate line 1, or P1, could have equal voltage as any Plate line shown in the figure).

Regarding claims 9 and 14, Kenney discloses in figure 1 a sense amplifier 14. Therefore, it would have obvious to one of ordinary skill in the art at the time of the invention to include this limitation in Yeh in order to sense the data in the bit line.

Response to Arguments

4. Applicant's arguments filed 3/12/03 have been fully considered but they are not persuasive.

Applicant primarily argues that the active area(s), indicated in the above rejections, does not operate as a bit line. Applicant therefore request that the examiner point out any portion of the Yeh reference to suggest or disclose that the active area(s) is a bit line, or operate as such.

The Office reminds the applicant that a bit line is a component of a device (normally a memory device) that two different voltage levels, low and high, are applied to it. The voltage levels are usually zero and five volts, or alternatively could be any voltage levels, as long as they are two separate voltage levels. Yeh reference discloses at column 10, lines 24-30; and lines 41-50, that when a data potential VBL is applied to the first substrate region 14, this potential is propagated to region 16, which in turn attains a high voltage. Conversely, when the voltage applied (VBL) is low, the potential of the active area(s) 16 is low. The voltage VBL is essential to the operation of the device (see column 10). Therefore, the active area(s), as defined in the above rejections, does in fact act as a bit line.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

Art Unit: 2814


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dana Farahani whose telephone number is (703)305-1914. The examiner can normally be reached on Monday-Friday 9:00AM - 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Dana Farahani
May 30, 2003



SUPERVISOR
TECHNICAL CENTER